ADAPTIVE EQUALIZATION METHODS AND APPARATUS FOR PROGRAMMABLE LOGIC DEVICES

Background of the Invention

[0001] This invention relates to programmable logic devices ("PLDs"), and more particularly to equipping PLDs with adaptive equalization capability.

[0002] PLDs are typically general-purpose integrated circuit devices that are designed to satisfy any of a wide range of user needs. The user does not have to design his or her own custom integrated circuit, subjecting himself or herself to the cost, delay, possible errors, and inflexibility of such a custom design. Instead, the user can immediately buy a commercially available, already proven PLD and program (configure) that device to perform whatever tasks the user needs to have performed. The PLD manufacturer does not know in advance all the details of all the uses various users may want to make of the PLD. But to give the PLD a reasonably large market to many different users (thereby helping to hold down the cost of the PLD by taking advantages of economies of scale), the manufacturer generally tries to equip a PLD with as

many capabilities as is reasonably possible within a broad target range of features for that particular PLD. Each user can then make use of the capabilities or features that the user needs and ignore the other capabilities or features.

[0003] PLDs are increasingly of interest for use in communication applications, especially those involving high speed data transmission. There are many different communication protocols and specifications that may be used (e.g., for communicating between devices in a system). If equipped with appropriate communication-supporting features, PLDs offer the possibility of being programmable to function in accordance with many different communication protocols and specifications.

[0004] Certain high speed communication protocols may require the receiver circuitry to provide equalization of the received signal (e.g., to compensate for such things as attenuation and/or phase shift of the signal in the course of transmission from the transmitter to the receiver). Any of several approaches may be taken to providing required equalization, and within each approach, different parameter values may need to be used, depending on the nature and extent of equalization that is called for. Moreover, because it is rarely the case that the exact amount of equalization that will be needed in a particular system or in a particular instance of a system will be known a priori, it is frequently desirable for the equalization capability that is provided to be "adaptive" (i.e., to be able to at least partly determine on an automatic or at least partly automatic basis the kind and/or amount of equalization needed in whatever instance is being served). It would

be desirable to provide a PLD with circuitry that can meet a wide range of equalization needs such as are referred to above.

Summary of the Invention

[0005] In accordance with the present invention, programmable logic device circuitry for adaptively equalizing a received data signal includes equalization circuitry that is programmable in at least some respect affecting one or more of the following aspects of the equalization circuitry: (1) the number of taps used, (2) whether integer or fractional spaced taps are used, (3) the starting values used for coefficient determination, (4) whether satisfactory coefficients are selected only once or on an on-going basis, (5) whether an error signal used is decision directed or based on a training pattern, (6) what training pattern (if any) is used, and/or (7) the location of the sampling point in the bit period of the signal to be equalized.

[0006] Methods in accordance with the invention include selecting various options with respect to one or more of the aspects mentioned in the preceding paragraph.

[0007] Further features of the invention, its nature and various advantages, will be more apparent from the accompanying drawings and the following detailed description.

Brief Description of the Drawings

[0008] FIG. 1 is a block diagram of an illustrative system that can be constructed in accordance with the invention.

[0009] FIG. 2 shows how FIGS. 3-5 are intended to be viewed together.

[0010] FIGS. 3-5 (viewed together as shown in FIG. 2) are collectively a simplified schematic block diagram of an illustrative embodiment of circuitry constructed in accordance with the invention.

[0011] FIG. 6 is a simplified block diagram of an illustrative larger system employing circuitry in accordance with the invention.

Detailed Description

[0012] An illustrative system 10 in accordance with the invention is shown in FIG. 1. System 10 includes transmitter circuitry 20 that transmits a signal (e.g., a high-speed digital data signal) to receiver circuitry 30 via lead 22. In the particular example shown in FIG. 1 receiver circuitry 30 is a programmable logic device ("PLD") with equalization capability in accordance with the invention. The equalization capability of PLD 30 is used to produce an equalized version of the signal received via lead 22. It will be understood that the equalization capability of PLD 30 may be only part of the capability and circuitry of the PLD, and that in addition to its equalization circuitry, PLD 30 may also have other circuitry and capability such as circuitry for making use of the equalized signal that is produced from the incoming signal on lead 22. Similarly, receiver circuitry 30 may include other components in addition to the depicted PLD. For example, the PLD portion of the receiver may be used (among other things) to produce an equalized version of incoming signal 22 for use by

other components that are part of a larger receiver subsystem 30.

[0013] FIGS. 3-5 show an illustrative embodiment of PLD 30 in more detail. As shown in FIG. 3 (and continued into FIGS. 4 and 5), PLD 30 includes equalization implementation circuitry 40, equalization control circuitry 50, and utilization and/or other circuitry 60. Equalization implementation circuitry 40 operates on incoming signal 22 to equalize it and thereby produce equalized signal 42. Circuitry 40 may be implemented using dedicated, special-purpose circuit elements (so-called "hard IP" (intellectual property)), or it may be implemented using more general-purpose circuit elements (e.g., programmable logic circuitry) that has been specially programmed (so-called "soft IP) to perform equalization tasks, or circuitry 40 may be implemented by a combination of hard and soft IP. Circuitry 40 includes a number of parts (e.g., 110, 120, etc.) that will be discussed in more detail later in this specification.

[0014] Equalization control circuitry 50 provides signals for controlling the various parts of circuitry 40. As part of providing such control signals, circuitry 50 may make signal selections and/or perform algorithms to determine what those control signals should be. One of the functions of circuitry 50 may be to compare the equalized signal to a reference signal to produce an error signal. Equalized signal 42 is an input to circuitry 50. Circuitry 50 includes a number of parts (e.g., 112, 114, 116, etc.) that will be discussed in more detail later in this specification. These various parts of

circuitry 50 may be implemented using hard IP, soft IP, or combinations thereof.

[0015] Utilization and/or other circuitry 60 may make any desired use of equalized signal 42 and/or it may pass on the equalized signal to other components (not shown) that are associated with (and thus in this respect served by) PLD 30.

[0016] The circuitry shown in FIGS. 3-5 can perform equalization of incoming signal 22 in any of one or more of several respects. These various respects will now be discussed in turn.

[0017] The first aspect of available equalization control is control of the number of taps that are included in the circuit performing the equalization. This aspect of the circuitry is implemented by element 110 in circuitry 40 and by elements 112, 114, 116, and 118 in circuitry 50. Element 110 implements how many taps are included in the circuit performing the equalization. One or more signals indicative of how many taps should be included are supplied to element 110 from the output(s) of multiplexer circuitry 114. (In general, throughout this specification (including the appended claims) references to a signal will be understood to include multiple signals and vice versa. The same is true for words like input and output. For example, a reference to outputs will be understood to also include the possibility that there may be only one output and vice versa. With that general understanding in mind, terminology used herein can be simplified by arbitrarily and interchangeably using either the singular or the plural of these kinds of terms. Occasionally a reminder that both singular and plural

possibilities are covered by use of either the singular or plural term may be provided. But omission of such an express statement does not negate the general rule that both singular and plural possibilities are covered by either form of reference.) Element 110 responds to the outputs of multiplexer circuitry 112 by putting into service in the equalization circuitry the number of taps indicated by those outputs.

[0018] Multiplexer circuitry 112 is controlled by programmable element 114 to get its outputs from either of its sets of inputs. Programmable element 114 may be a RAM bit that is programmed when PLD 30 is configured (e.g., by the user). The same is true for the other programmable elements that are described later in this specification. (These programmable elements are another example of components that can be provided in any number, so that any reference herein to either single or plural programmable elements will be understood to include both single and plural configurations as possibilities.) The first selectable set of inputs to multiplexer circuitry 112 are the outputs of programmable elements 116. The second selectable set of inputs to multiplexer circuitry 112 are the outputs of element 118. Programmable elements 116 allow the user to dictate the number of taps that will be used. To do this, the user programs elements 116 to indicate the desired number of taps, and the user programs element 114 to cause multiplexer circuitry 112 to select the outputs of elements 116 for application to element 110. Alternatively, the user can program circuitry 112 to select the outputs of element 118 for application to element 110. Element 118 is circuitry for performing what is called a "number of

taps control algorithm." This algorithm can be any algorithm for automatically determining how many taps should be used based on whatever criteria it is desired to consider. For example, this algorithm may start with a low number of taps. If satisfactory equalization cannot be achieved, the algorithm may gradually increase the number of taps until satisfactory equalization is achieved.

[0019] Examples of why it is desirable in a PLD to provide the foregoing flexibility regarding the number of taps used and the ways in which that number can be determined are as follows. The range of possible users of and applications for a PLD are wide. Thus it is desirable to provide programmability in the number of taps used for equalization. A very attenuated medium 22 may require more taps to equalize properly. On the other hand, short backplanes or cables can reduce adaptation time (time required to determine what equalization is required) and power consumption by reducing the number of taps.

[0020] Element 118 may itself have some elements of programmability. For example, a user may be able to programmably specify the number of taps that the algorithm of element 118 will start with and/or the maximum number of taps that the algorithm may attempt to use. As another example, element 118 may be capable of performing two or more different algorithms for determining the number of taps to be used, and the user may programmably select which algorithm will be used.

[0021] The second aspect of available equalization control is selection of use of integer spaced taps or fractional spaced taps in the circuit performing the equalization. Integer spaced taps effectively operate

on the incoming signal at the symbol rate (i.e., once per symbol period) or an integer multiple of the symbol period of the incoming signal. Fractional spaced taps effectively operate on the incoming signal at some multiple of (e.g., 2, 3, 4, etc., times) the symbol rate. (The symbol rate and the symbol period are reciprocally related to one another. The last sentence before this parenthetical is therefore the same as saying that the fractional spacing of the taps is 1/2, 1/3, 1/4, etc. of the symbol period or bit period of the incoming data signal 22.) Elements 120, 122, 124, 126, and 128 implement this aspect of equalization control.

[0022] Element 120 (in circuitry 40) implements whether integer or fractional taps are used by the circuitry performing the equalization. In addition, element 120 typically implements what integer is used in the case of integer taps and what fraction is used in the case of fractional taps. Element 120 is controlled by the outputs of multiplexer circuitry 122 (in circuitry 50).

[0023] Multiplexer circuitry 122 is controlled by programmable element 124 to select either of its selectable input sets for application to element 120. One of these selectable input sets comes from programmable elements 126. The other selectable input set comes from element 128. Elements 126 allow the user to specify whether integer or fractional spaced taps will be used, and possibly also what integer or what fraction will be used. Alternatively, element 128 performs an algorithm for automatically or at least partly automatically making these determinations based on any criteria that it is desired to consider.

[0024] There may be some programmable aspects to the operation of element 128. For example, element 128 may be capable of implementing two or more different algorithms, and the user may be able to make a programmable selection of which algorithm may be used. As another example, the user may be able to programmably select an integer limit or limits, or a fraction limit or limits that element 128 must observe.

[0025] Because a PLD may be expected to be able to support a wide range of data rates, it can be an advantage to provide the ability to support either fractional or integer spaced taps as described above.

[0026] A third aspect of available equalization control has to do with how the starting values for equalization function coefficients are determined. This aspect is implemented by elements 130, 132, 134, 136, 138, and 140 (FIG. 4).

[0027] Element 130 (in circuitry 40) stores the coefficient values that are used in the circuitry performing the equalization. These coefficient values are determined by coefficient computation algorithm 132 (in circuitry 50). Starting values for these coefficients are supplied via the outputs of multiplexer circuitry 134. This circuitry is controlled by programmable element 136 to get its outputs from either programmable elements 138 or from coefficient starting value algorithm 140. In this way the user can either specify the coefficient starting values (using programmable elements 138) or allow the circuitry to automatically or at least partly automatically determine the coefficient starting values (using element 140).

[0028] As in the case of other equalization aspects discussed above, there may be programmable aspects to element 140. For example, the user may be able to specify limits within which element 140 is to operate.

[0029] It is desirable to provide the coefficient starting value options described above. A good guess programmed in by the user can greatly reduce adaptation time. On the other hand, if the user cannot provide a good guess, then it may be preferable to use element 140, because a bad starting point may lead to longer adaptation time or perhaps never converging on a solution.

[0030] Typically a coefficient value cannot exceed plus or minus 1 (+/-1) because coefficients are normalized with respect to the main bit. It is therefore necessary to provide enough RAM bits 138 and algorithm 140 output bus width to adequately represent a fraction between +/-1 for each coefficient.

[0031] A fourth aspect of available equalization control relates to the choice of how to generate an error signal for use whenever such a signal is needed in the equalization adaptation process. The options provided are decision directed error signal algorithm 164 and an algorithm 166 for error signal generation using a training pattern. The user can select either of these options by programming programmable element 162 to control multiplexer circuitry 160 to derive the error signal from the desired source (164 or 166).

[0032] This aspect of the circuitry allows the user to select whether a training pattern is available. Using a training pattern can greatly speed up convergence and improve the accuracy of the algorithm.

On the other hand, some users may not be able to tolerate sending a training pattern. So having a decision directed alternative available allows PLD 30 to support a wider range of users.

[0033] A fifth aspect of available equalization control relates to allowing a user who is able to supply a training pattern for use during adaptation of the equalization to specify and change the training pattern. This aspect is implemented by elements 170, 172, 174, and 176. A predetermined training pattern is stored in element 176. A user who wants to can store a different training pattern in programmable elements 174. The user programs programmable element 172 to control multiplexer circuitry 170 to supply to element 166 either the training pattern from element 176 or the training pattern from elements 174.

[0034] A sixth aspect of available equalization control relates to whether PLD 30 performs one equalization adaptation cycle or continues to adapt the equalization to possible changes in the environment. This aspect is implemented by programmable element 150, which the user can program to tell element 132 whether to stop and lock in the coefficient values that have been determined when the adaptation algorithm is first completed, or to continue to operate to adjust the coefficient values in the event that the equalization needed changes in any respect. Continuous or on-going calibration may consume more power, but it allows the adaptive equalizer to continuously monitor line 42 (FIG. 3) for any changes that may require new coefficients. Element 132 would then supply those new coefficients to element 130.

[0035] A seventh aspect of available equalization control relates to determining the location of the sampling point in the bit period of incoming signal 22. This aspect is implemented by elements 180, 182, 184, 186, and 188 (FIG. 5).

[0036] Element 180 (in circuitry 40) controls where in the incoming signal bit period that signal is sampled for use in the equalization circuitry tap(s). Because PLD 30 is preferably designed to support a wide range of data rates, extending into very high frequencies, a particular sampling point location may not be optimal in all cases. The aspect of the circuitry now being described allows the sampling to be moved to fine tune its placement. Elements 182, 184, 186, and 188 allow the user to use either a sampling location determined at least partly automatically by an algorithm 188 implemented by the circuitry, or to specify a sampling location by appropriately programming programmable elements 188. The user programs programmable element 184 to cause multiplexer circuitry 182 to pass the outputs of element 188 on to element 180 if the user wants element 188 to select the sampling location. Alternatively, the user programs element 184 to cause multiplexer circuitry 182 to pass the outputs of elements 186 on to element 180 if the user wants element 180 to use a sampling location the user has specified.

[0037] It should be understood that all embodiments of the invention do not necessarily include all of the above-described aspects of equalization control. It is also within the scope of the invention to use any one or more of the above-described aspects.

[0038] FIG. 6 illustrates a PLD 30 of this invention in a data processing system 202. Data processing system 202 may also include one or more of the following components: a processor 204; memory 206; I/O circuitry 208; and peripheral devices 210. These components (including PLD 30) are coupled together by a system bus or other interconnections 220 and are populated on a circuit board 230 (e.g., a printed circuit board) that is contained in an end-user system 240. Any of the connections to element 30 from any other element(s) may make use of the adaptive equalization capability of PLD 30. Similarly, additional instances of programmable logic circuitry with adaptive equalization capability in accordance with the invention may be included in any of the other system components so that those components can also have the benefits of the invention in processing signals they receive.

[0039] System 202 can be used in a wide variety of applications, such as computer networking, data networking, instrumentation, video processing, digital signal processing, or any other application where the advantage of using programmable or reprogrammable logic is desirable. PLD 30 can be used to perform a variety of different logic or other functions. For example, PLD 30 can be configured as a processor or controller that works in cooperation with processor 204. PLD 30 may also be used as an arbiter for arbitrating access to a shared resource in system 202. In yet another example, PLD 30 can be configured as an interface between processor 204 and one of the other components in system 202. It should be noted that system 202 is only exemplary, and that the true scope and spirit of

the invention should be indicated by the following claims.

[0040] Various technologies can be used to implement PLDs 30 having the features of this invention, as well as the various components of those devices (e.g., the programmable function control elements ("FCEs") such as elements 114 and 116 in FIG. 3 and the like). For example, FCEs can be SRAMs, DRAMs, first-in first-out ("FIFO") memories, EPROMs, EEPROMs, function control registers (e.g., as in Wahlstrom U.S. patent 3,473,160), ferro-electric memories, fuses, antifuses, or the like. From the various examples mentioned above it will be seen that this invention is applicable to both one-time-only programmable and reprogrammable devices.

[0041] It will be understood that the foregoing is only illustrative of the principles of the invention, and that various modifications can be made by those skilled in the art without departing from the scope and spirit of the invention. For example, the underlying adaptive equalization circuitry and techniques used (exclusive of features added by the present invention) can be any suitable known circuitry and techniques. As illustrations of this point, the algorithms referred to in elements 118, 128, 132, 140, 164, 166, and 188 can be any suitable known algorithms. In the appended claims it is sometimes said that various parameters are "computed" or determined by "computing." This type of language generally parallels use of the term "algorithm" in the accompanying FIGS. and the above discussion. It will be understood, however, such computing may take any of many forms, including the use of look-up tables or the like. Another way to state

this point is that look-up tables or the like are among the techniques that are referred to herein as algorithms.